

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for operating a constant current circuit, comprising:
after connecting a sampling capacitor connected between a gate and a source of a first transistor and a drain of the first transistor to a reference current source and setting a voltage across the sampling capacitor to a voltage between the gate and the source produced while the first transistor is driven by a reference current of the reference current source,
cutting off the connection among the sampling capacitor, the first transistor and the reference current source, as well as connecting the drain of the first transistor to a driving target, and driving the driving target by a current of the first transistor due to the voltage between the gate and the source that is set in the sampling capacitor,
wherein said cutting off the connection comprises applying a first signal to a gate of a second transistor connected between the drain of the first transistor and the reference current source,
and
a second signal ~~that is opposite said first signal~~that is a logical inverse of said first signal to a gate of a third transistor connected between the gate and drain of the first transistor, and
a third signal to a gate of a fourth transistor connected between the drain of the first transistor and the driving target.

2. (Previously Presented) The method for operating a constant current circuit according to claim 1, further comprising:

repeating a period for setting the voltage across the sampling capacitor and a period for driving the driving target.

3. (Currently Amended) A flat display device constructed so that a display section made of pixels arranged in a matrix form, a vertical driving circuit for sequentially selecting the pixels of the display section through gate lines, and a horizontal driving circuit for driving pixels selected through the gate lines, by signal lines of the display section,
characterized in that:

the horizontal driving circuit comprises:

a digital-to-analog conversion circuit for performing digital-to-analog conversion processing of gradation data indicative of gradations of the pixels; and

a buffer circuit for driving the signal lines by means of an output signal from the digital-to-analog conversion circuit;

the buffer circuit drives the signal lines by a source follower circuit formed by connecting a constant current circuit to a source of a transistor; and

the constant current circuit is configured such that, after connecting a sampling capacitor connected between a gate and a source of a first transistor and a drain of the first transistor to a reference current source and setting a voltage across the sampling capacitor to a voltage between the gate and the source produced while the first transistor is driven by a reference current of the reference current source, cuts off the connection among the sampling capacitor, the first transistor and the reference current source, as well as connects the drain of the first transistor to a driving target and drives the driving target by a current of the first transistor due to the first voltage between the gate and the source that is set in the sampling capacitor,

wherein said cutting off the connection comprises applying a first signal to a gate of a second transistor connected between the drain of the first transistor and the reference current source, and

a second signal that is opposite said first signal that is a logical inverse of said first signal to a gate of a third transistor connected between the gate and drain of the first transistor, and

a third signal to a gate of a fourth transistor connected between the drain of the first transistor and the driving target.

4. (Previously Presented) The flat display device according to claim 3, wherein the constant current circuit is configured for repeating a period for setting the voltage across the sampling capacitor and a period for driving the driving target, the period for setting the voltage across the sampling capacitor being set as a period for precharge of the display section.

5. (Currently Amended) A constant current circuit, comprising:

a first transistor having a gate, a source, and a drain, the drain of the first transistor being configured for selective connection to a reference current source;

a sampling capacitor configured for selective connection between the gate and the source of the first transistor, for setting a voltage across the sampling capacitor to a voltage between the gate and the source produced while the first transistor is driven by a reference current of the reference current source,

wherein the drain of the first transistor is selectively connected to a driving target after setting said voltage across the sampling capacitor, for driving the driving target by a current of the transistor due to the voltage between the gate and the source that is set in the sampling capacitor;

~~a first signal applied to a gate of a second transistor having a gate, a source, and a drain, connected between the drain of the first transistor and the reference current source~~ the drain of the second transistor being configured to selectively connect the first transistor and the reference current source,

wherein the gate of the fourth transistor is configured to receive a first signal that enables the selective connection of the first transistor and the reference current source; and

~~a second signal that is opposite said first signal applied to a gate of a third transistor having a gate, a source, and a drain, connected between the gate and drain of the first transistor~~ the third transistor being configured to set the voltage across the sampling capacitor,

wherein the gate of the third transistor is configured to receive a second signal that is a logical inverse of said first signal and that enables the setting of the voltage across the sampling capacitor; and

a fourth transistor having a gate, a source, and a drain, the fourth transistor being configured to selectively connect the driving target and the drain of the first transistor,

wherein the gate of the fourth transistor is configured to receive a third signal that enables the selective connection of the driving target and the drain of the first transistor.

6. (Previously Presented) The constant current circuit according to claim 5, wherein a period for setting the voltage across the sampling capacitor and a period for driving the driving

target are repeated, the period for setting the voltage across the sampling capacitor being set as a period for pre-charge of a display section.